REMARKS

INTRODUCTION

Claims 1-18 were previously pending and under consideration.

Claims 1, 3 and 5 are cancelled herein.

Claim 19 is added herein.

Therefore, claims 2, 4, and 6-19 are now pending and under consideration.

Claims 1-18 are rejected.

Claims 2, 4, 6, 7 and 10-18 are amended herein.

No new matter is being presented, and approval and entry are respectfully requested.

ENTRY OF AMENDMENT UNDER 37 CFR §1.116

Applicant requests entry of this Rule 116 Response because:

(a) it is believed that the amendment of the claims puts this application into condition for allowance;

(b) the amendments were not earlier presented because the Applicant believed in good faith that the cited prior art did not disclose the present invention as previously claimed;

(c) the amendments of the claims should not entail any further search by the Examiner since no new features are being added or no new issues are being raised; and

(d) the amendments do not significantly alter the scope of the claims and place the application at least into a better form for purposes of appeal. No new features or new issues are being raised.

The Manual of Patent Examining Procedures sets forth in Section 714.12 that "any amendment that would place the case either in condition for allowance or in better form for appeal may be entered." Moreover, Section 714.13 sets forth that "the Proposed Amendment

should be given sufficient consideration to determine whether the claims are in condition for allowance and/or whether the issues on appeal are simplified." The Manual of Patent Examining Procedures further articulates that the reason for any non-entry should be explained expressly in the Advisory Action.

REJECTIONS UNDER 35 USC § 102

In the Office Action, at pages 2-8, claims 1-18 were rejected under 35 U.S.C. § 102 as anticipated by Losq. This rejection is traversed and reconsideration is requested.

CLAIMS 6, 7, 10, 13, AND 19

Claim 6 recites branch prediction, when the return occurs, when the register number of the branch destination address register corresponds to a branch destination address register, such as register 14, which is commonly designated as the branch destination address register. The portion of Losq noted by the Examiner (Losq page 2, lines 2-8) discusses instructions, not registers. Losq does not address this feature.

Claim 7 recites features such that the push onto the stack is not being performed when the register number of the link register corresponds to a branch destination address register, such as register 14, which is commonly designated as the branch destination address register. Losq and ESA/390 Principles of Operation discuss nothing being pushed onto the stack when the register is zero. Nothing is said about not pushing when the register is the commonly used branch destination address register. As a result, Losq does not address this feature.

Claim 10 relates to invalidating of the contents of the storing circuit when a non-correspondence event occurs, such as an interrupt. Losq does not address this feature. The rejection pointed to page 2, line 44-page 3, line 1 of Losq for this feature. This portion of Losq does not address this invalidating feature.

Claim 13 recites features relating to an ability to perform branch prediction when the instruction equivalent to a call instruction, such as the microcode executed bassm instruction, is not registered in the branch history. Losq requires that the branch instruction be of the type that is registered in the branch history table (BHT). That is a BHT hit is required for Losq to make a

not registered in the branch history. Losq requires that the branch instruction be of the type that is registered in the branch history table (BHT). That is a BHT hit is required for Losq to make a prediction for a return instruction, such as the microcode executed BSM instruction, that may be an instruction equivalent to a subroutine return. See also new claim 19.

Withdrawal of the rejection of claims 6, 7, 10, and 13, and allowance of new claim 19, is respectfully requested.

CLAIMS 4, 8, 9, 11, 12, AND 14-18

Claim 1 recites "an identifying circuit identifying an instruction equivalent to a subroutine return, which corresponds to the instruction equivalent to the subroutine call". Claim 1 recites applicability to "instruction equivalent to subroutine returns and corresponding to instructions to equivalent to subroutine calls". See figure 6, and in particular the instructions of BCR, BAL, and BALR. Therefore, claim 1 differs from Losq because it is applicable to any of the register-relative-branch instructions that represent instructions to equivalent to subroutine returns and in correspondence with instructions equivalent to subroutine calls.

According to claims 8, 9, 11, and 12, execution of an instruction is controlled by treating the instruction as an instruction equivalent to a subroutine return. For example, if the instruction is found as R1=1 and R2=14 with respect to its BALR, and as an instruction equivalent to a subroutine call if found otherwise with respect to the BALR (R2≠ 0), and consequently, a higher success rate than with Losq is possible. According to Losq, an instruction is decoded and an associated result is registered as a data set indicating whether the instruction is a BCR (BCR/NOT A BCR), and whether the instruction is a BAL, BALR, or neither (BAL/BALR/NEITHER). This is in contrast to the present invention where a registered flag implies a SUBROUTINE_CALL or a SUBROUTINE_RETURN. The flag differs from Losq, and this type of control is not possible with Losq. Furthermore, Losq cannot handle a register-relative-branch instruction that, while not constituting any BAL, BALR or BCR, represents an instruction that is equivalent to either a subroutine call or subroutine return. Unlike Losq, the invention of claims 8, 9, 11, and 12 can handle any instruction of the type discussed above.

Claim 4 recites "only the taken instruction of a branch instruction is thus registered". In

instruction execution process at an RSBR, both BRHIS and RETURN_ADRS_STACK are updated simultaneously in a manner so directed by an instruction issued from the branch instruction-execution-processing unit. Claims 14-18 recite a similar feature.

Withdrawal of the rejection of claims 4 and 14-18 is respectfully requested.

DEPENDENT CLAIMS

The dependent claims are deemed patentable due at least to their dependence from allowable independent claims. These claims are also patentable due to their recitation of independently distinguishing features. For example, claim 12 recites that the predicting circuit does not use a popped return address as a predicted branch destination. This feature is not taught or suggested by the prior art. Withdrawal of the rejection of the dependent claims is respectfully requested.

CONCLUSION

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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